What is claimed is:

1. A semiconductor package comprising:

a first chip defining an active surface and having a high-frequency element defining a high-frequency area on the active surface;

a substrate supporting the first chip and electrically connected to the first chip;

a middle layer disposed on the first chip and having a recess corresponding to the high-frequency area; and

a second chip disposed on the middle layer and electrically connected to one of the first chip and the substrate.

2. The semiconductor package as claimed in claim 1, further comprising an encapsulant encapsulating the first chip, the middle layer, the second chip, and a part of the substrate.

3. The semiconductor package as claimed in claim 1, wherein the substrate further comprises a plurality of solder balls for electrically connecting an external circuit.

4. The semiconductor package as claimed in claim 1, further comprising:

a plurality of bonding wires for electrically connecting the first chip to the substrate.

5. The semiconductor package as claimed in claim 1, further comprising:

a plurality of bonding wires for electrically connecting the second chip to the first chip.

6. The semiconductor package as claimed in claim 1, further comprising:

a plurality of bonding wires for electrically connecting the second chip to the substrate.

7. The semiconductor package as claimed in claim 1, wherein the recess is a through hole.

8. A semiconductor package comprising:

a chip defining an active surface and having a high-frequency element defining a high-frequency area on the active surface;

a substrate supporting the chip;

a plurality of bumps for electrically connecting the chip to the substrate; and

an encapsulant encapsulating the active surface of the chip, the bumps, and a part of the substrate, and having a cavity positioned below the high-frequency area.

9. The semiconductor package as claimed in claim 8, wherein the substrate further has a plurality of solder balls for electrically connecting an external circuit.

10. The semiconductor package as claimed in claim 8, wherein the cavity is formed through the encapsulant.

11. The semiconductor package as claimed in claim 10, wherein the substrate further has a notch corresponding to the cavity.

12. A semiconductor package comprising:

a chip defining an active surface and having a high-frequency element defining a high-frequency area on the active surface;

a substrate supporting the chip and electrically connected to the chip;

an encapsulant encapsulating the active surface of the chip, and a part of the substrate; and

a cavity positioned within the encapsulant above the high-frequency area.

13. The semiconductor package as claimed in claim 12, wherein the substrate further has a plurality of solder balls for electrically connecting an external circuit.

14. The semiconductor package as claimed in claim 12, further comprising:

a plurality of bonding wires for electrically connecting the chip to the substrate.